IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicant(s): Andreas Klug
Appl. No.: 09/647,431
Conf. No.: 8643
Filed: October 2, 2000
Title: METHOD AND APPARATUS FOR COUPLING AN ATM COMMUNICATION LAYER TO A PLURALITY OF TIME-DIVISION MULTIPLEX COMMUNICATION TERMINALS
Art Unit: 2662
Examiner: Donald L. Mills
Docket No.: 112740-112

Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

RESPONSE TO OFFICE ACTION

Sir:

The present remarks are in response to the office action entered in the above identified case and mailed on November 5, 2003. Claims 11-20 are pending in the application. Claims 11, 12 and 15-20 were rejected under 35 U.S.C. §102(b) and claims 13 and 14 were rejected under 35 U.S.C. §103, all in light of the disclosure of Yamada et al. in U.S. Patent No. 5,412,655. Applicants respectfully traverse.

Yamada does not disclose, teach, or suggest all of the elements in any of the currently pending claims. Accordingly, the pending claims are neither anticipated by nor obvious over Yamada et al.

Independent claim 11 of the present application calls for a method of coupling an Asynchronous Transfer Mode (ATM) communication layer to a plurality of time-independent time-division multiplex communication terminals. The method includes the step of generating a control signal sequence having a clock rate corresponding to the overall cell rate CR_N of the time-division multiplex communication terminals. The control signal sequence may take on one of two states. ATM cells are transmitted from the ATM communication layer into an ATM cell waiting list or queue. ATM cells are transmitted, on demand, to a requesting time-division multiplex communication terminals. An ATM cell is transmitted from the end of the queue

when a corresponding oldest signal in the control signal sequence represents a first of the two states that the control signal may take on. In contrast, a fixed data pattern is transmitted to the requesting time-division multiplex communication terminal when the oldest control signal of the control signal sequence represents the second of the two states that the control signal may take on. The oldest control signal of the control signal sequence is then deleted.

Claim 20 is similar, but calls for an apparatus for coupling an ATM communication layer to a plurality of mutually time-independent time division-multiplex communication terminals. In this claim a generator is called for for generating a control signal sequence such as that described above with regard to the method of claim 11. A first transmitter transmits ATM cells coming from the ATM communication layer into an ATM cell waiting list. A second transmitter transmits an ATM cell from the ATM cell waiting list to a requesting time-division multiplex communication terminal when the oldest control signal of the control signal sequence represents a first state, and transmitting a fixed data pattern when the oldest control signal of the control signal sequence represents a second state. The oldest control signal of the control signal sequence is then deleted.

These features are not disclosed by Yamada et al. Yamada et al. disclose a multiprocessing system for assembly/disassembly of asynchronous transfer mode cells. (See title) The cell disassembly is comprised of a cell accumulation unit, a cell disassembly control unit, a memory controller, a buffer memory and a plurality of additional address memories (Col. 5, lines 1-8). Payload data from received ATM cells are stored in the buffer memory. Data are read out of the buffer memory in units of a TDM fixed bit rate for each channel specified on the basis of the frame and clock pulses of an output TDM data highway (Col. 5, lines 55-61.)

Upon receiving an ATM cell, the cell accumulation controller writes the payload data of the cell on an unused bank of the buffer memory and makes a time series chain structure of the bank addresses on an FCBA memory (First Cell Bank Address), an LBCA memory (Last Cell Bank Address) and an address chain memory, for each logical channel col. 6, lines 2-9. The cell disassembly control unit disassembles the payload data of the first cell of the chain structure for a logical channel specified by the logical channel converter into TDM data. The TDM data are transferred from an internal clock to the clock of the TDM data highway by the clock converter

and are transferred to the data. If there is not cell disassembled, then idle data are output from the idle data transmission controller. (Col. 6 lines 22-30).

This is the extent of Yamada et al.'s relevant disclosure relied on by the Examiner in rejecting the claims pending in the present application. Note, nowhere do Yamada et al. describe generating a control signal sequence with a clock rate corresponding to the overall payload cell rate of N time division multiplex communication terminals. For this step of claim 11 the Examiner points to Yamada et al. Fig. 1 and col. 5 lines 54-59. According to the Examiner, Yamada et al.'s disassembly control unit controls the buffer memory, and inherently comprises a clock rate that is compatible with the TDM data highway and controls the transmission of cells or idle traffic. This statement is true enough, but it does not teach what is being claimed. Yamada et al. col. 5 lines 54-59 states that the cell disassembly unit controls the buffer memory and the address memories "such that data is read out from the bank storing the payload data in units of the TDM fixed bit rate data for each virtual channel specified on the basis of the frame pulse and clock of the TDM data highway." Thus, data are read out of buffer the memory according to the TDM data highway bit rate and according to the TDM data highway frame structure. This is not the same as a control signal sequence having a clock rate corresponding to the overall payload cell rate CR_N of N time-division multiplex communication terminals.

Furthermore, Yamada et al. do not disclose teach or suggest transmitting ATM cells from an ATM cell waiting list when a respective oldest control signal of the control signal sequence represents a first status, and transmitting a fixed data pattern when the respective oldest control signal of the control signal sequence represents a second status, then deleting the oldest control signal of the control signal sequence. As described above, Yamada et al. do not disclose, teach or suggest generating such a control signal sequence. Thus, they cannot possibly disclose, teach or suggest transmitting either ATM cells or a fixed data pattern based on the control signal status of the Non-disclosed control signal sequence, then deleting the oldest non-existent control signal. Yamada et al. do teach transmitting idle data when there is not ATM cell present to transmit. However, they teach nothing in regard to how such a determination is made. Stating that it is inherently based on the status of the oldest control signal of a control signal sequence having a clock rate corresponding to the overall payload cell rate of a plurality of time division multiplex terminals is a matter of pure conjecture on the part of the Examiner.

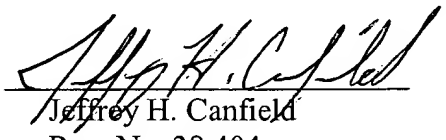
Since Yamada et al. do not disclose, teach or suggest all of the features of the independent claims pending in the present application, the rejections under 35 U.S.C. §102(b) and §103 are improper and should be withdrawn. The dependent claims are allowable for the same reasons.

For these reasons, Applicant respectfully submits that the claims as they presently stand are all in condition for allowance. Applicant therefore requests that the Examiner allow the claims move the application to issue. However, if there are any remaining issues the Examiner is encourage to call Applicants' attorney, Jeffrey H. Canfield at (312) 807-4233 in order to facilitate a speedy disposition of the present case.

If any additional fees are required in connection with this response they may be charged to deposit account no. 02-1818.

Respectfully submitted,

BELL, BOYD & LLOYD LLC

BY 

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